WHAT IS CLAIMED IS:

1. A driver comprising:

a p-channel MOS transistor having a p+ source connected to a supply voltage, a p+ drain connected to a first node, a gate, and an n-bulk connected to a second node;

an n-channel MOS transistor having an n+ source connected to ground, an n+ drain connected to the first node, a gate, and a p-bulk connected to a p-bulk voltage;

a gate signal generator that outputs a PMOS gate signal to the gate of the p-channel MOS transistor, an NMOS gate signal to the gate of the n-channel MOS transistor, and a control signal, the PMOS and NMOS gate signals being non-overlapping;

a first switch connected to ground, the control signal, and the n-bulk of the p-channel MOS transistor via the second node;

a second switch connected to ground and the control signal; and

a resistor that is connected to the n-bulk of the p-channel MOS transistor, a current flowing through the resistor to ground when the second switch is closed, and not flowing when the second switch is open.

2. The driver of claim 1 wherein the control signal has a logic state opposite to the logic state of the PMOS gate signal.

3. The driver of claim 1 and further comprising:

a third switch connected to the second switch and the resistor that is controlled by an enable signal; and

a fourth switch connected to the voltage source and the resistor that is controlled by the enable signal.

4. The driver of claim 1 wherein the p+ source includes a plurality of p+ strips formed in the n-bulk, a p+ source strip having a width that varies with length from a first width to a second larger width to the first width.

5. The driver of claim 4 wherein the p+ drain includes a plurality of p+ strips formed in the n-bulk, a p+ drain strip having a width that varies with length from a third width to a fourth smaller width to the third width.

6. The driver of claim 5 wherein a first line normal to the lengths of the p+ source strip and the p+ drain strip passes through the first width and the third width, the third width being larger than the first width.

7. The driver of claim 6 wherein a second line normal to the lengths of the p+ source strip and the p+ drain strip passes through the second width and the fourth width, the second width being larger than the first width.

8. The driver of claim 7 and further comprising a plurality of first channel region strips, a first channel region strip located between adjacent p+ source and drain strips, the first channel region strip having a shape that varies with length, the shape being defined by the adjacent n+ source and drain strips; and

a plurality of first gate strips, a first gate strip formed over each first channel region strip, the first gate strip having a shape that varies with length and substantially matches the shape of the first channel region strip.

9. The driver of claim 8 and further comprising:
a region of field oxide; and
an interconnect line formed on the region of field oxide.

10. The driver of claim 9 wherein each end of a gate strip is connected to the interconnect line.

11. The driver of claim 8 wherein the n+ source includes a plurality of n+ strips formed in the p-bulk, an n+ source strip having a width that varies with length from a fifth width to a sixth larger width to the fifth width.

12. The driver of claim 11 wherein the n+ drain includes a plurality of n+ strips formed in the p-bulk, a n+ drain strip having a width that varies with length from a seventh width to an eighth smaller width to the seventh width.

13. The driver of claim 12 wherein a third line normal to the lengths of the n+ source strip and the n+ drain strip passes through the fifth width and the seventh width, the seventh width being larger than the fifth width.

14. The driver of claim 13 wherein a second line normal to the lengths of the n+ source strip and the n+ drain strip passes

through the sixth width and the eighth width, the sixth width being larger than the eighth width.

15. The driver of claim 14 and further comprising a plurality of second channel region strips, a second channel region strip located between adjacent n+ source and drain strips, the channel region strip having a shape that varies with length, the shape being defined by the adjacent n+ source and drain strips; and

a plurality of second gate strips, a second gate strip formed over each second channel region strip, the second gate strip having a shape that varies with length and substantially matches the shape of the second channel region strip.

16. The driver of claim 15 and further comprising:

a plurality of first contacts electrically connected to the p+ source and drain strips; and

a plurality of second contacts electrically connected to the n+ source and drain strips, the first contacts being larger than the second contacts.

17. The driver of claim 15 wherein:

the n+ source strips have a first maximum width; and

the n+ drain strips have a second maximum width that is larger than the first maximum width.

18. A method of driving a signal with a driver, the driver having:

a p-channel MOS transistor having a p+ source connected to a supply voltage, a p+ drain connected to a first node, a gate, and an n-bulk connected to a second node;

an n-channel MOS transistor having an n+ source connected to ground, an n+ drain connected to the first node, a gate, and a p-bulk connected to a p-bulk voltage;

a first switch connected to ground, the control signal, and the n-bulk of the p-channel MOS transistor via the second node;

a second switch connected to ground and the control signal; and

a resistor that is connected to the n-bulk of the p-channel MOS transistor, a current flowing through the resistor to ground when the second switch is closed, and not flowing when the second switch is open,

the method comprising the steps of:

turning off the n-channel MOS transistor;

turning on the p-channel MOS transistor after the n-channel MOS transistor has been turned off; and

connecting the n-bulk to ground via the resistor when the p-channel MOS transistor is on.

19. The method of claim 18 and further comprising the steps of:

turning off the p-channel MOS transistor;

connecting the n-bulk to a voltage greater than ground when the p-channel transistor is off; and

turning on the n-channel MOS transistor.

20. A MOS transistor comprising:

a plurality of first strips of a first conductivity type, a first strip having a width that varies with length from a first width to a second larger width to the first width;

a plurality of second strips of the first conductivity type, a second strip having a width that varies with length from a third width to a fourth smaller width to the third width, a line normal to the lengths of the first strip and the second strip passes through the first width and the third width, the third width being larger than the first width;

a plurality of channel region strips, a channel region strip located between adjacent first and second strips, the channel region strip having a shape that varies with length, the shape being defined by the adjacent first and second strips; and

a plurality of gate strips, a gate strip formed over each channel region strip, the gate strip having a shape that varies with length and substantially matches the shape of the channel region strip.